Patent claims

1. A method for fabricating a semiconductor memory element arrangement, which has the following steps:
   - application of a first electrically insulating layer on a substrate;
   - application of a layer system comprising a floating gate and a tunnel barrier arrangement applied on the floating gate on the first insulating layer;
   - formation of a first gate electrode adjacent to the floating gate, via which gate electrode electrical charge can be fed to the floating gate or can be dissipated from the latter, and a second gate electrode adjacent to the tunnel barrier arrangement, via which second gate electrode it is possible to control the electrical charge transmission of the tunnel barrier arrangement;
   - the first and second gate electrodes being formed in a first trench structure formed in the layer system, which first trench structure comprises first trenches arranged parallel to one another and extending as far as the first insulating layer, and a second trench structure formed in the layer system, which second trench structure comprises second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the first insulating layer.

2. The method as claimed in claim 1, in order to form the first and second trench structures, a second electrically insulating layer being applied on the tunnel barrier arrangement and patterned in accordance with the first and second trench structures.

3. The method as claimed in claim 2, the patterning of the second electrically insulating layer applied on the tunnel barrier arrangement having the following steps:
   - performance of a first photolithography step using a first photomask having a pattern of parallel strip-type openings whose width corresponds to the minimum feature size; and
   - performance of a second photolithography step using a second photomask having a pattern of parallel strip-type openings which are arranged perpendicular to the strip-type openings of the first photomask and whose width corresponds to the minimum feature size.

4. The method as claimed in claim 3, after the first photolithography step and before the second photolithography step, spacers being formed on the second insulating layer in the first trenches.

5. The method as claimed in one of the preceding claims, the first trenches having a smaller width than the second trenches.

6. The method as claimed in one of the preceding claims, the first and second gate electrodes being formed as spacers in the second trenches of the second trench structure.

7. The method as claimed in one of the preceding claims, the step of forming the first gate electrode in the first and second trench structures having the following steps:
   - application of a third electrically insulating layer on the sidewalls of the first and second gate structures;
   - application of a first polysilicon layer on the third electrically insulating layer with filling of the width of the first trenches and formation

of first polysilicon spacers in the second trenches in order to form the first gate electrode.

8. The method as claimed in one of the preceding claims, the step of forming the second gate electrode in the first and second trench structures having the following steps:
- application of a fourth electrically insulating layer on the first polysilicon layer;
- application of a second polysilicon layer on the third and fourth electrically insulating layers with filling of the width of the first trenches and formation of second polysilicon spacers in the second trenches in order to form the second gate electrode.

9. The method as claimed in one of the preceding claims, the first, second, third and fourth electrically insulating layers being formed from silicon nitride or silicon dioxide.

10. The method as claimed in one of the preceding claims, the first and second gate electrodes being formed from polysilicon.

11. The method as claimed in one of the preceding claims, the tunnel barrier arrangement being formed as a layer stack with an alternating layer sequence of semiconducting and insulating layers for the purpose of forming a multiple tunnel barrier.

12. The method as claimed in claim 11, the semiconducting layers of the layer stack being formed from undoped polysilicon.

13. The method as claimed in claim 11 or 12, the insulating layers of the layer stack being formed from silicon nitride or silicon dioxide.

14. The method as claimed in one of claims 11 to 13, the semiconducting layers of the layer stack being formed with a thickness in the range of 30 to 50 nm and the insulating layers being formed with a thickness in the range of 2 to 4 nm.

15. The method as claimed in one of claims 11 to 13, the semiconducting layers of the layer stack being formed with a thickness and also a grain size of at most 2 nm and the insulating layers being formed with a thickness of at most 1.5 nm.

16. A method for operating a semiconductor memory element arrangement having a first electrically insulating layer applied on a substrate and a layer system comprising a floating gate and a tunnel barrier arrangement applied on the floating gate, said layer system being applied on the first electrically insulating layer;

- the electrical potential on the floating gate being read via a first gate electrode; and
- the electrical charge transmission of the tunnel barrier arrangement being controlled via a second gate electrode,
- the first and second gate electrodes being formed in a first trench structure formed in the layer system, which first trench structure comprises first trenches arranged parallel to one another and extending as far as the first insulating layer, and a second trench structure formed in the layer system, which second trench structure comprises second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the first insulating layer.

17. The method as claimed in claim 16, for reading data of the semiconductor memory element arrangement, an electrical voltage being applied to the first gate electrode with the second gate electrode free of voltage.

18. The method as claimed in claim 16 to 17, for writing or erasing data of the semiconductor memory element arrangement, an electrical voltage being applied to the second gate electrode with the first gate electrode free of voltage.

19. A semiconductor memory element arrangement, in which a plurality of semiconductor memory elements are arranged in a matrix-like manner in a plurality of rows and columns, each semiconductor memory element having

- a first electrically insulating layer applied on a substrate,
- a layer system comprising a floating gate and a tunnel barrier arrangement applied on the floating gate, said layer system being applied on the first electrically insulating layer;
- a first gate electrode adjacent to the floating gate and serving for determining the charge carriers stored in the floating gate;
- and a second gate electrode adjacent to the tunnel barrier arrangement, via which gate electrode it is possible to control the charge transmission of the tunnel barrier arrangement;
- the first and second gate electrodes being formed in a first trench structure formed in the layer system, which trench structure comprises first trenches arranged parallel to one another and extending as far as the first insulating layer, and a second trench structure formed in the layer system, which trench structure comprises second trenches arranged parallel to

one another and perpendicular to the first trenches and extending as far as the first insulating layer.